1 Digital Interface

Pin	Direction	Function
SCK	in	SCK for SPI communication/SCK for PLL communication
MOSI	in	MOSI for SPI communication/MOSI for PLL communication
MISO	out	MISO for SPI communication/MUX for PLL communication
NSS	in	Chip Select for SPI communication/LE for PLL communication
INTR	out	Active high interrupt indicator
RESET	in	FPGA reset
AUX1	in	Selector for direct communication with Source PLL
AUX2	in	Selector for direct communication with LO PLL
AUX3	in	Active low modulation enable. Should be high when changing settings

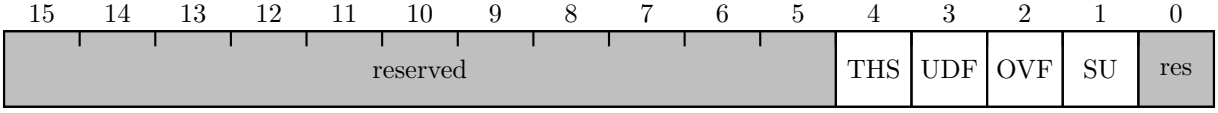
Depending on the voltage on AUX1/AUX2 the SPI port controls either the FPGA or one of the MAX2871 PLLs:

AUX1	AUX2	Function
low	low	SPI communication with FPGA
high	low	Direct feedthrough of SCK, MOSI, MISO and NSS to Source PLL
low	high	Direct feedthrough of SCK, MOSI, MISO and NSS to LO PLL
high	high	Invalid

When communicating with a PLL, the MUX output of the MAX2871 is forwarded to MISO and the NSS signal is forwarded to the LE pin. As the LE pin should stay low until after a valid register has been shifted in (see MAX2871 datasheet), set NSS low before switching to PLL communication mode.

2 SPI Protocol

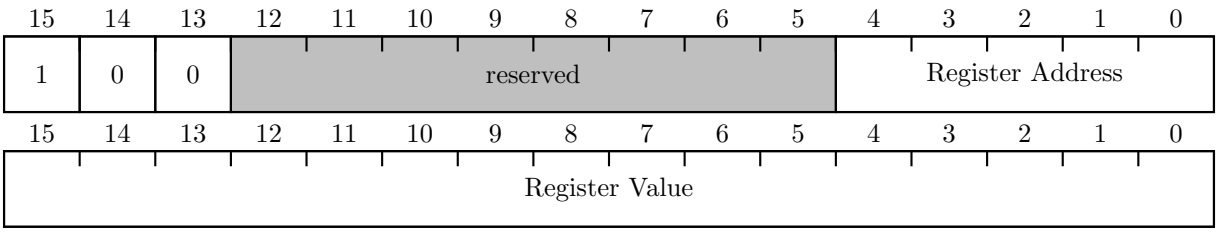
Each SPI transfer starts with pulling NSS low and ends with NSS returning to high level. SPI communication is done in words of 16 bits. The first word after NSS is pulled low is the command word and determines the amount and meaning of the following words. The word received while transmitting the command word is the interrupt status register:



- **THS:** Threshold of modulation FIFO reached. See also section 2.3. Reset on its own when the FIFO level drops again.
- **UDF:** Modulation FIFO underflow. Last sample will be used for modulation until new data arrives. Reset as a new sample is added to the FIFO.
- **OVF:** Modulation FIFO overflow. Oldest sample will be overwritten. Reset by disabling the modulation.
- **SU:** Source unlocked

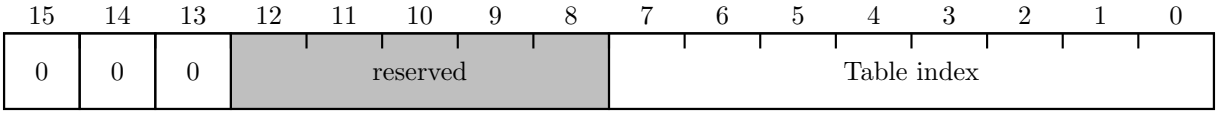
2.1 Writing a register

Writing a register requires the transfer of two words: First the control word selecting the destination address and a second word containing the new register value:

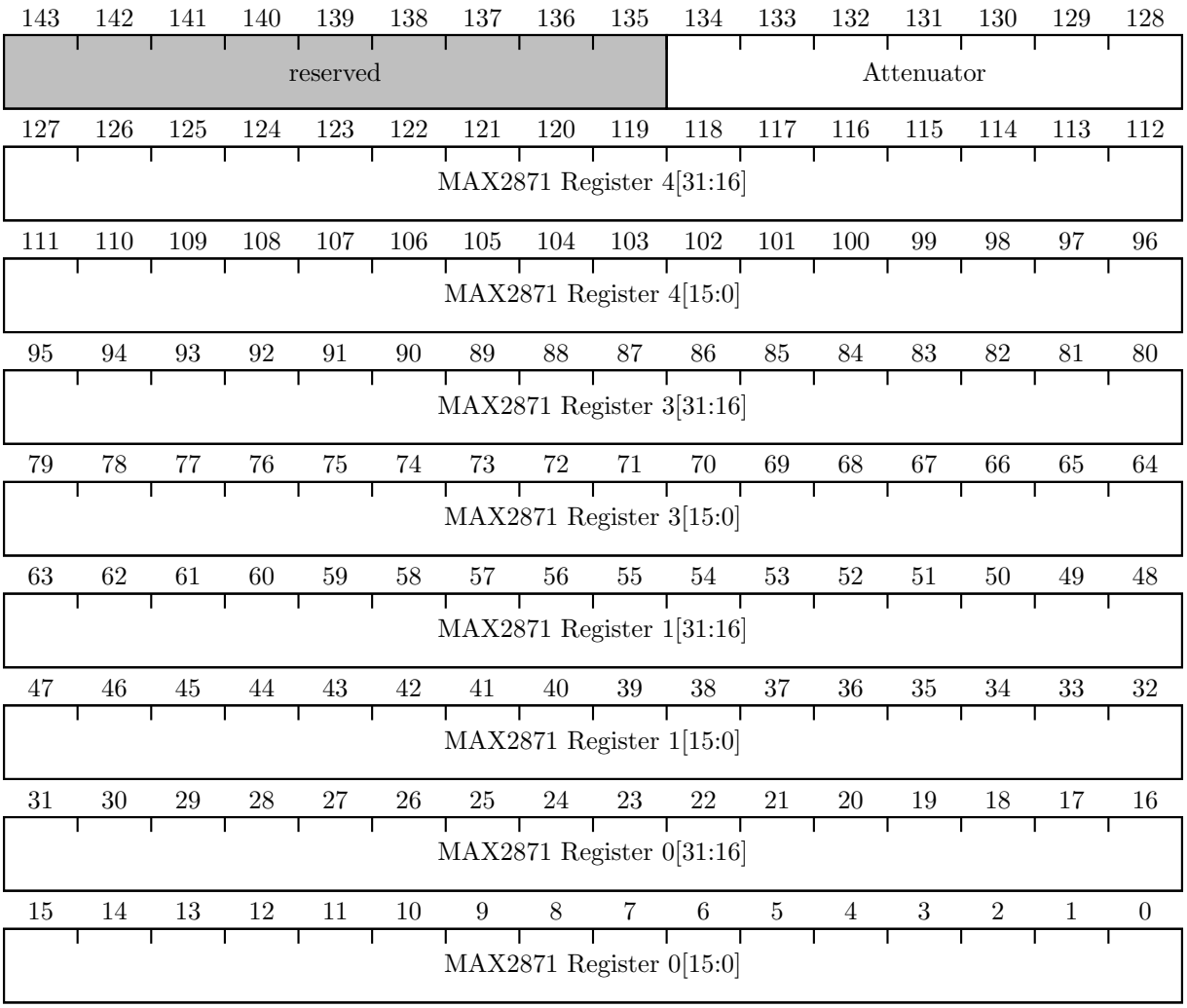


2.2 Writing to the modulation lookup table

The source registers and the attenuator setting are taken from a lookup table while the modulation is active. There is one entry for every possible value of the sample (256 entries). All used entries must have been written to before the modulation is started. Initiate the write by sending the command word:



While keeping NSS low, send the lookup table data after the control word. The data is only written to the table, when all 9 words have been received. The data is transmitted MSB first.



2.3 Modulation FIFO handling

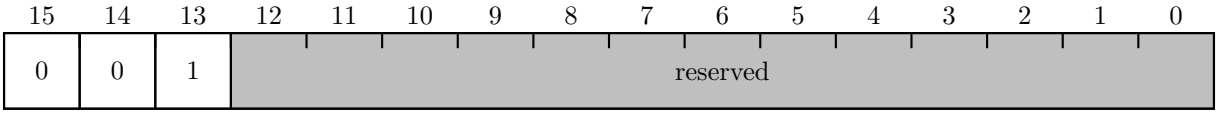
The modulation module contains a data FIFO for the modulation data (samples). Each sample is an 8-bit word that determines the modulation state. The modulation moves on to the next sample at a rate determined by MOD_PHASE_INC. The FIFO has a size of 2048 samples. It can only be written to, reading back data from the FIFO is not possible.

The FIFO also has three interrupts (see status register, section refreg:status):

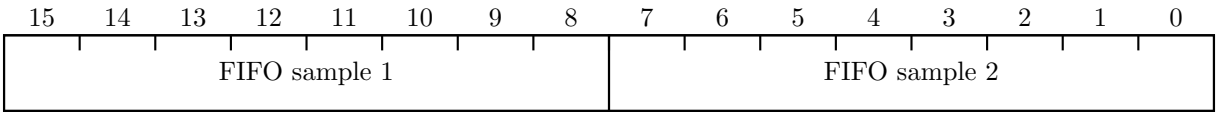
- **Overflow:** Asserted when samples have been written to an already full FIFO. This bit does not clear even if the FIFO level drops afterwards. The modulation has to be disabled to reset this bit. Disabling the modulation also clears the FIFO.
- **Underflow:** Asserted when no more samples are available in the FIFO but the modulation module is scheduled to move to the next sample. The modulation will continue to use the last available sample until new data is written to the FIFO. This bit is cleared by writing new FIFO data.
- **Threshold crossed:** Asserted when the FIFO contains at least MOD_FIFO_THRESHOLD (see section refreg:mod:fifo:thresh) samples.

2.3.1 Writing to the modulation FIFO

It is only possible to write to bytes at a time to the modulation FIFO. Initiate the write by sending the command word:



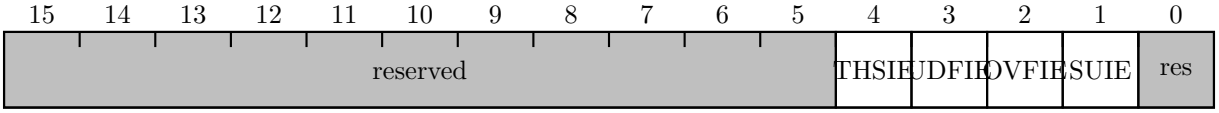
Follow up the same SPI transaction (NSS has to stay low) with as many words as desired, each word containing two FIFO samples:



FIFO sample 1 is added to the FIFO first, followed by FIFO sample 2.

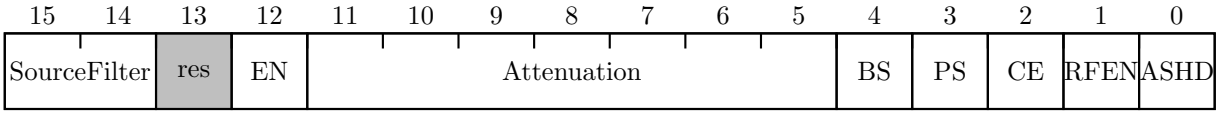
3 Registers

3.1 Interrupt Mask Register: 0x00



- **THSIE:** FIFO threshold crossed interrupt enable
- **UDFIE:** FIFO underflow interrupt enable
- **OVFIE:** FIFO overflow interrupt enable
- **SUIE:** Source unlocked interrupt enable

3.2 Control Register: 0x01

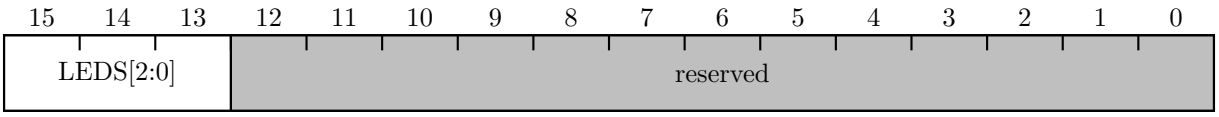


- **SourceFilter:** Low pass filter selection for source signal

Setting	Selected Band
00	0 MHz to 900 MHz
01	900 MHz to 1800 MHz
10	1800 MHz to 3500 MHz
11	3500 MHz to 6000 MHz

- **EN: Enable modulation.** Set to 1 to enable the modulation. For the modulation to actually start, AUX3 also has to be pulled low. Set to 0 to disable the modulation (when changing settings or to clear the modulation FIFO).
- **Attenuator:** Attenuation of source signal in 0.25 dB (when modulation is disabled).
- **BS: Band select.** Set to 0 for highband, set to 1 for lowband.
- **PS: Port select.** Set to 0 for Port 1, set to 1 for Port 2.
- **CE: Source chip enable.**
- **RFEN: Source RF enable.**
- **ASHD: Amplifier disable.**

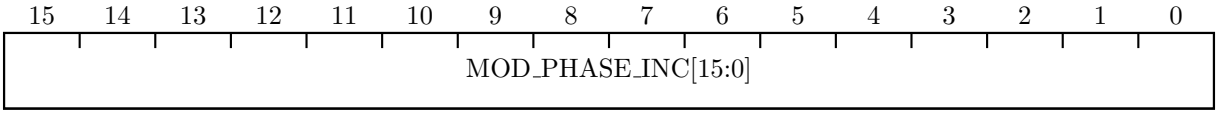
3.3 LED control register: 0x02



- **LEDS:** User LED status:

LED num	Function
0	Debug
1	Ready
2	Ext. reference

3.4 Modulation phase increment register: 0x03

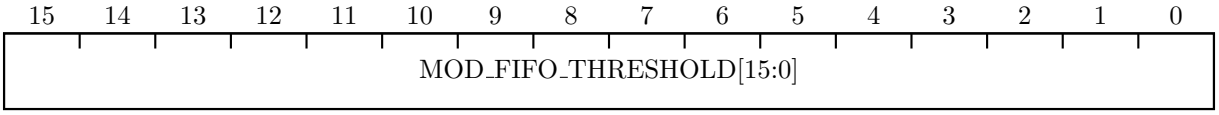


Determines the rate at which the modulation module consumes samples:

$$f_{sample} = \frac{102.4MHz * MOD\_PHASE\_INC}{2^{27}}$$

Example: set to 26214 for a sample rate of approximately 20 kHz.

3.5 Modulation FIFO threshold register: 0x04



- **MOD_FIFO_THRESHOLD[15:0]:** Number of samples in the FIFO after which the FIFO threshold interrupt is asserted.