1 Digital Interface

Pin	Direction	Function
SCK	in	SCK for SPI communication/SCK for PLL communication
MOSI	in	MOSI for SPI communication/MOSI for PLL communication
MISO	out	MISO for SPI communication/MUX for PLL communication
NSS	in	Chip Select for SPI communication/LE for PLL communication
INTR	out	Active high interrupt indicator
RESET[1]	in	FPGA reset
AUX1	in	Selector for direct communication with Source PLL
AUX2	in	Selector for direct communication with LO PLL
AUX3	in	Active low sweep enable. Has to be high when changing settings
Trigger In[2]	in	Trigger input for synchronization across devices
Trigger Out[3]	Out	Trigger output for synchronization across devices

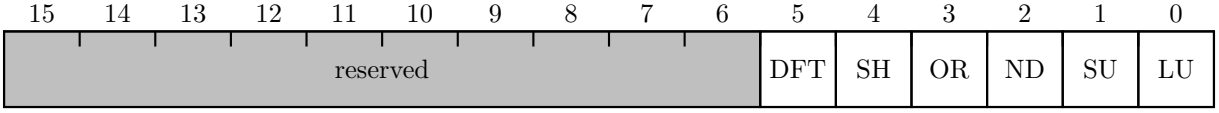
Depending on the voltage on AUX1/AUX2 the SPI port controls either the FPGA or one of the MAX2871 PLLs:

AUX1	AUX2	Function
low	low	SPI communication with FPGA
high	low	Direct feedthrough of SCK, MOSI, MISO and NSS to Source PLL
low	high	Direct feedthrough of SCK, MOSI, MISO and NSS to LO PLL
high	high	Invalid

When communicating with a PLL, the MUX output of the MAX2871 is forwarded to MISO and the NSS signal is forwarded to the LE pin. As the LE pin should stay low until after a valid register has been shifted in (see MAX2871 datasheet), set NSS low before switching to PLL communication mode.

2 SPI Protocol

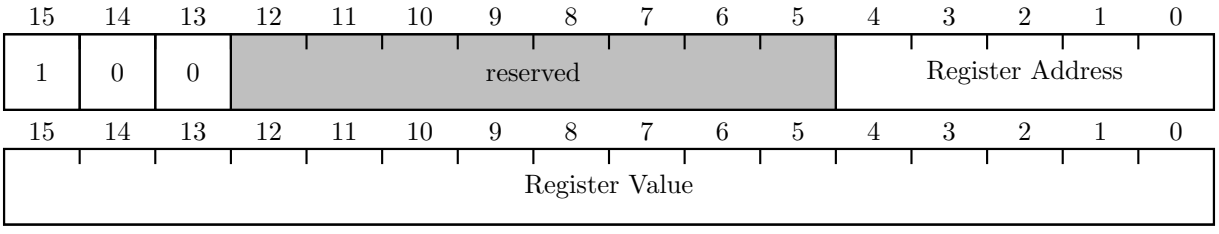
Each SPI transfer starts with pulling NSS low and ends with NSS returning to high level. SPI communication is done in words of 16 bits. The first word after NSS is pulled low is the command word and determines the amount and meaning of the following words. The word received while transmitting the command word is the interrupt status register:



- **DFT:** New DFT result available (see section 3.10).
- **SH:** Sweep halted due to halt bit set. Sweep will be resumed once the resume command is issued.
- **OR:** Data overrun occured (only cleared by resetting the FPGA)
- **ND:** New data available
- **SU:** Source unlocked
- **LU:** LO unlocked

2.1 Writing a register

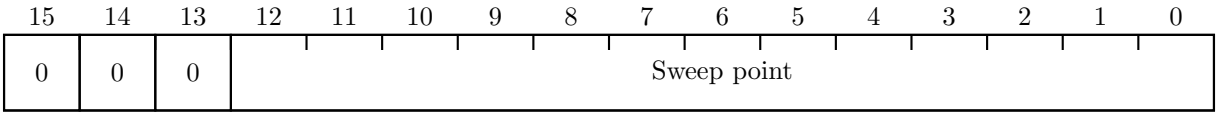
Writing a register requires the transfer of two words: First the control word selecting the destination address and a second word containing the new register value:



[1]Reset is named "MCU_FPGA_UNUSED1" in the schematic as this is a later software addition
[2]Trigger In is named "MCU_FPGA_UNUSED2" in the schematic as this is a later software addition
[3]Trigger Out is named "MCU_FPGA_UNUSED3" in the schematic as this is a later software addition

2.2 Writing SweepConfig

Initiate the sweep config transfer by sending the command word:

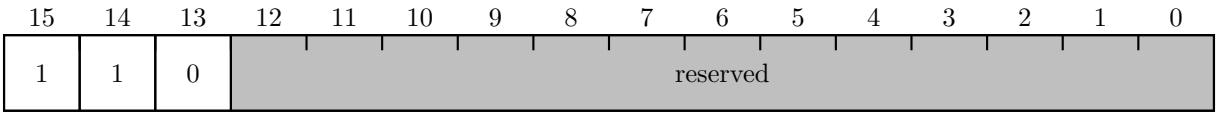


The maximum number of points per sweep is 4501, thus the highest valid value for "Sweep point" is 4500. After the control word, send the six words of the sweep config (see section 4) while keeping NSS low. The sweep config is transmitted MSB first.

2.3 Reading a sampling result

Whenever the ND bit in the interrupt status register is set, new sampling data is available and can be read via SPI. It has to be read before the next sampling data arrives otherwise the old data will be overwritten.

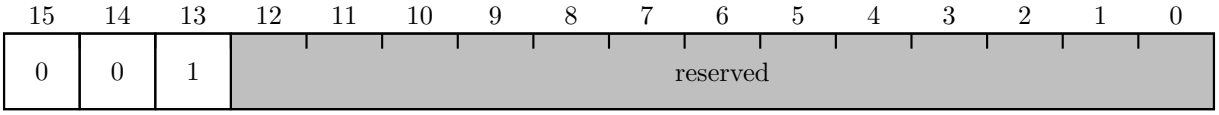
Initiate the reading of sampling data by sending the command word:



Afterwards, read up to 19 words before setting NSS high. These 19 words will contain the sampling result (see section 5), transmitted with the least significant word first.

2.4 Resuming a halted sweep

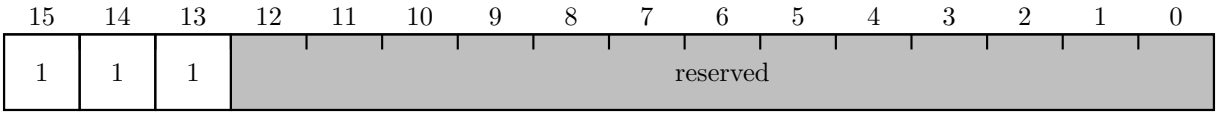
When the halt bit is set in the SweepConfig, the FPGA will configure the Source and LO as requested but will not start the settling timer (and subsequently the sampling process) until this resume command is issued. The halted sweep is indicated by the sweep halted bit in the status register.



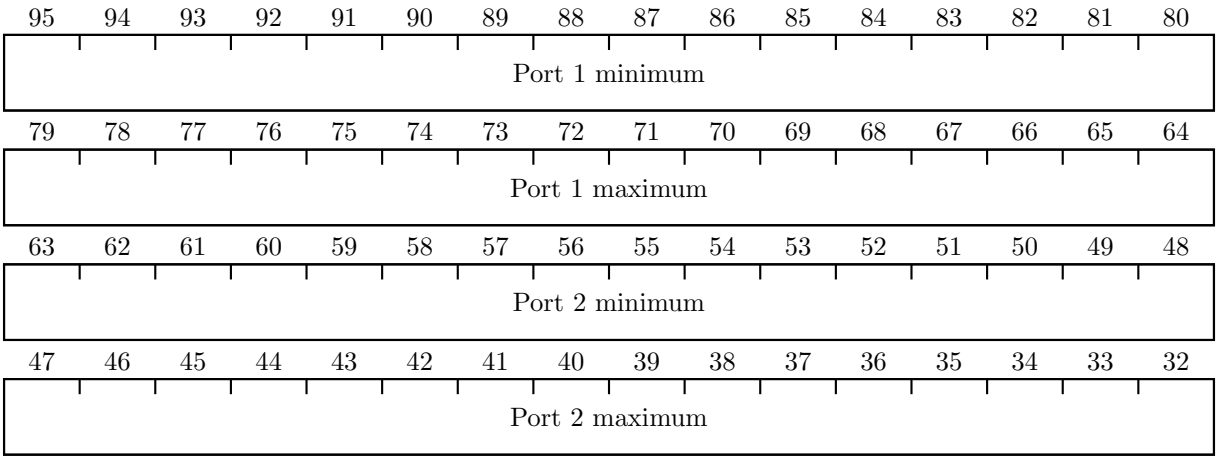
2.5 Reading ADC limits

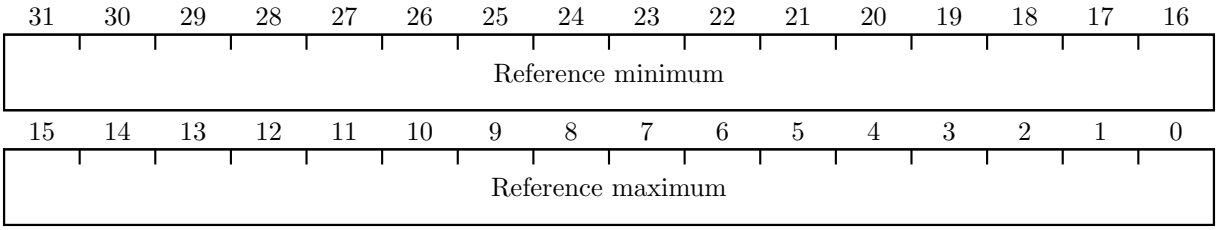
The FPGA keeps track of the highest and lowest sample of each ADC to detect saturation and verify signal levels.

Initiate the reading of ADC limit data by sending the command word:



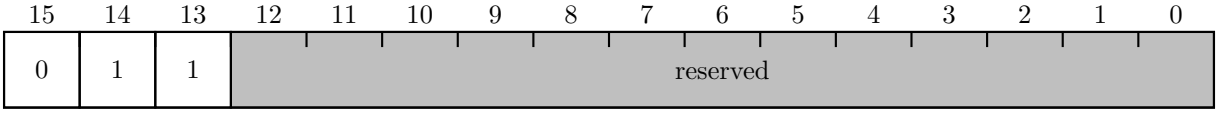
Afterwards, read 6 words before setting NSS high. These 6 words will contain the sampling result:





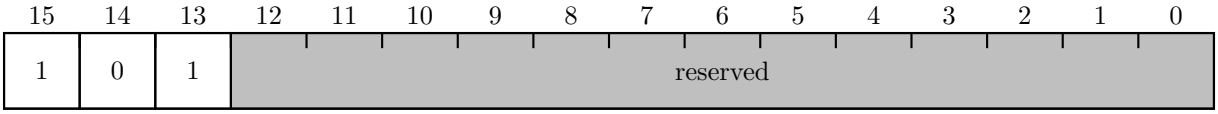
2.6 Resetting the ADC limit

Issuing this command result in all minimum values set to 32767 and all maximum values set to -32768.

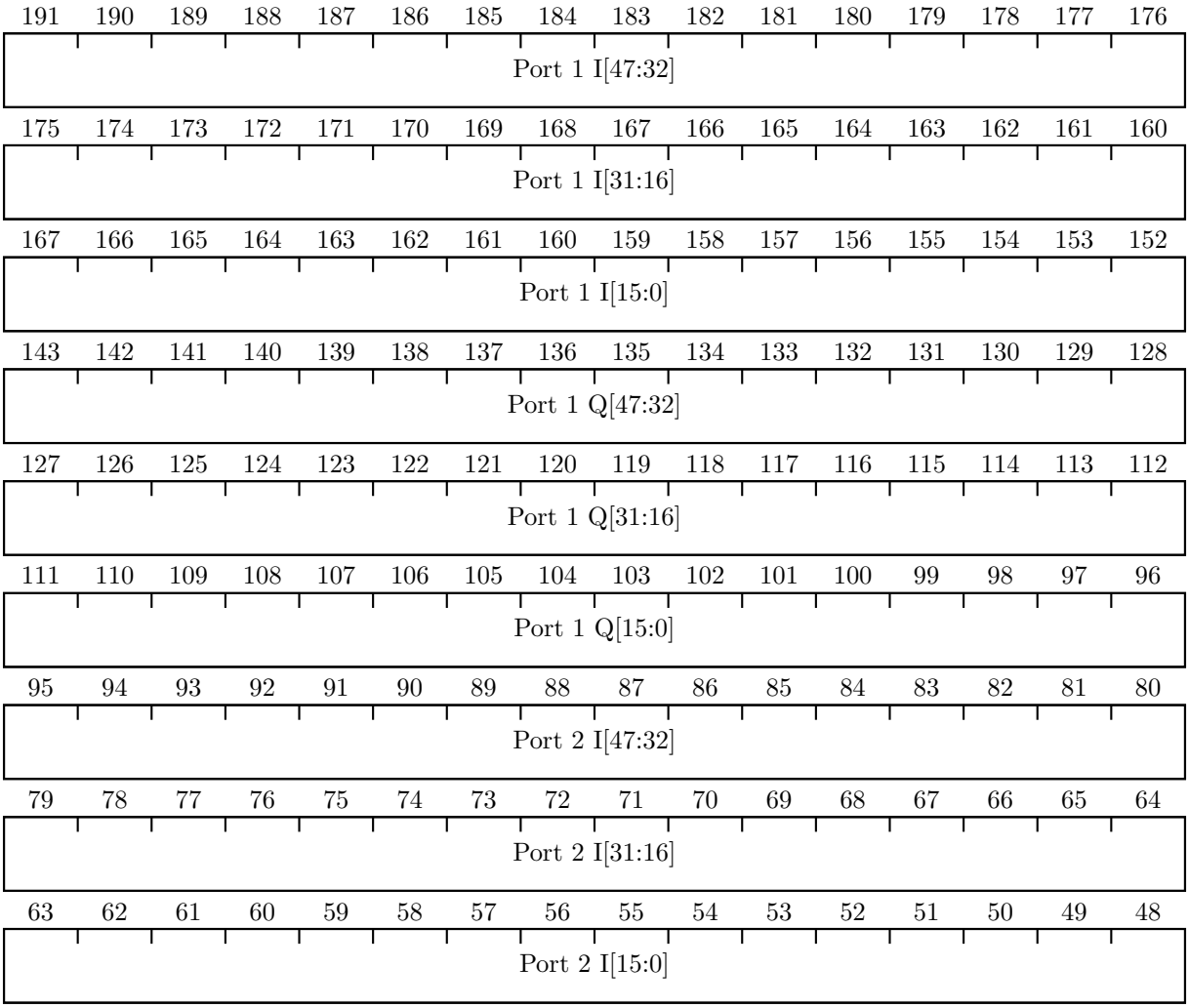


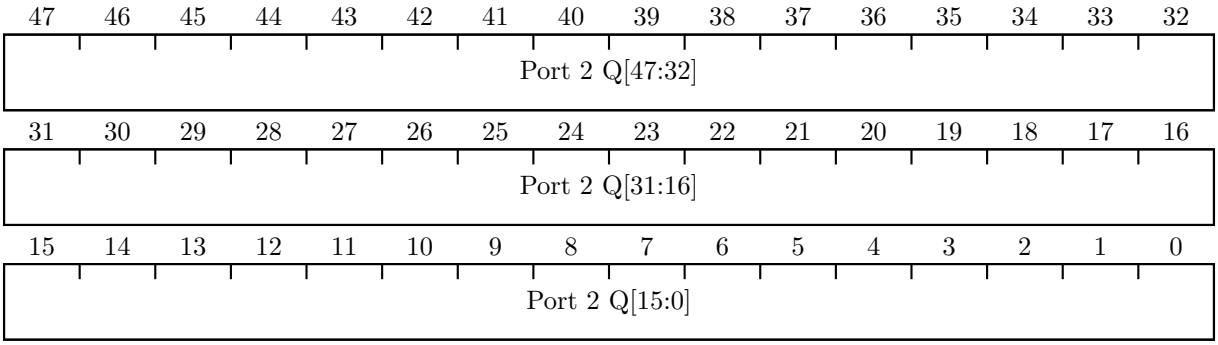
2.7 Reading the DFT result

Initiate the reading of the DFT result (see section 3.10) by sending the command word:



Afterwards, read 12 words before setting NSS high. These 12 words will contain the first bin of the DFT, the least significant word is transmitted first:

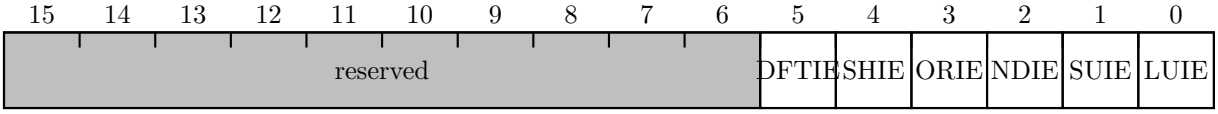




Repeating this procedure will return the next DFT bin. For each bin, the CS pin has to be toggled and the command word needs to be sent again (each DFT bin requires a new SPI transaction). The DFT interrupt is reset once all bins have been read. Alternatively, toggling the DFT off and on (by disabling and enabling its interrupt) will also reset the interrupt flag.

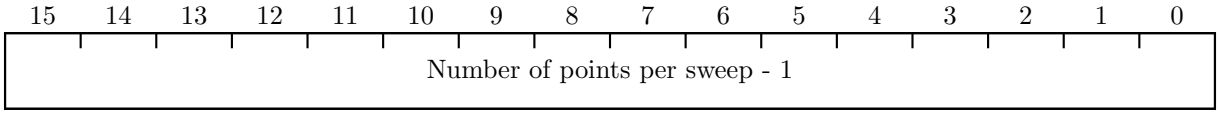
3 Registers

3.1 Interrupt Mask Register: 0x00



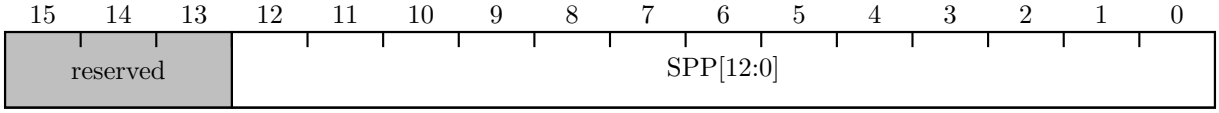
- **DFTIE:** DFT interrupt enable. This bit also enables the DFT (see section 3.10).
- **SHIE:** Sweep halted interrupt enable
- **ORIE:** Data overrun interrupt enable
- **NDIE:** New data interrupt enable
- **SUIE:** Source unlocked interrupt enable
- **LUIE:** LO unlocked interrupt enable

3.2 Sweep Points Register: 0x01



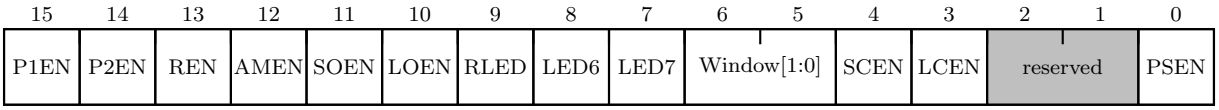
The register contains the number of points per sweep negative one, e.g. set to 11b if the sweep contains four points.

3.3 Samples Per Point Register: 0x02



- **SPP[12:0]:** The register contains the number of samples per point in increments of 16 samples (e.g. SPP=0b0000001000=0x08 uses 128 samples per point). The value of this register is only used if SweepConfig[92:90] is set to 000. Otherwise it is overwritten for the sweep point with one of seven preselected values.

3.4 System Control Register: 0x03

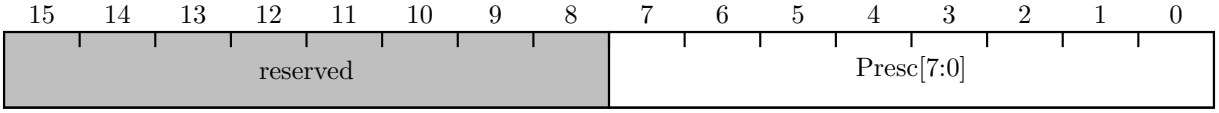


- **P1EN:** Port 1 Mixers/Amplifier enable
- **P2EN:** Port 2 Mixers/Amplifier enable
- **REN:** Reference Mixers/Amplifier enable
- **AMEN:** Source amplifier enable
- **SOEN:** Source enable
- **LOEN:** LO enable
- **RLED:** External frequency LED control
- **LED6:**User LED 6 control
- **LED7:**User LED 7 control
- **Window[1:0]:**Type of window to be used in calculation of real/imag of the sampling result

Setting	Window type
00	Rectangular (no window)
01	Kaiser
10	Hann
11	Flat Top

- **SCEN:**Source chip enable
- **LCEN:**LO chip enable
- **PSEN:**Port switch enable

3.5 ADC Prescaler register: 0x04

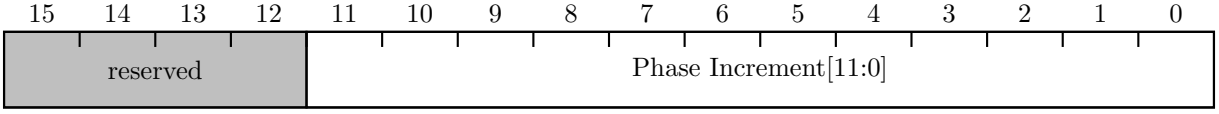


- **Presc[7:0]:** Amount of FPGA clock cycles between ADC samples.

$$SR_{ADC} = \frac{102.4\,\text{MHz}}{Presc}$$

The minimum value for this register is 112, which results in a samplerate of roughly 914.3 kHz. If Presc is set to a lower value, the data acquisition from the ADC is not done when the next sample starts and samples will be skipped.

3.6 Phase Increment: 0x05



- **Phase Increment[7:0]:** Phase angle between ADC samples for DFT bin calculation in $\frac{2\pi}{4096}$rad. For a given ADC samplerate SR_{ADC} and final IF frequency f_{IF2} set this value to

$$PhaseInc = \frac{4096 * f_{IF2}}{SR_{ADC}}$$

For the the default IF frequency of $f_{IF2} = 250\,\text{kHz}$ this evaluates to 10*Presc (see ADC prescaler register).

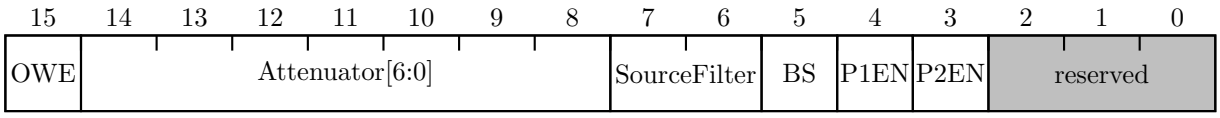
3.7 Sweep setup: 0x06

Each point in the sweep is done in stages. Each stage consists of (optionally) routing the source signal to one of the ports and sampling of all ADCs. A "new data" interrupt is triggered after each stage.

- **Stages** Number of stages per point - 1. Normally the number of stages is equal to the number of ports but it can also be less (e.g. if only S11 is measured).
- **SYNC:** Enables synchronization mode (see section 6).
- **Port 1 stage** Number of stage during which the source signal is routed to port 1. Must not have the same value as Port 2 stage.
- **Port 2 stage** Number of stage during which the source signal is routed to port 2. Must not have the same value as Port 1 stage.

3.8 Hardware override register: 0x07

Allows overwriting hardware settings, regardless of whether a sweep is active or not.



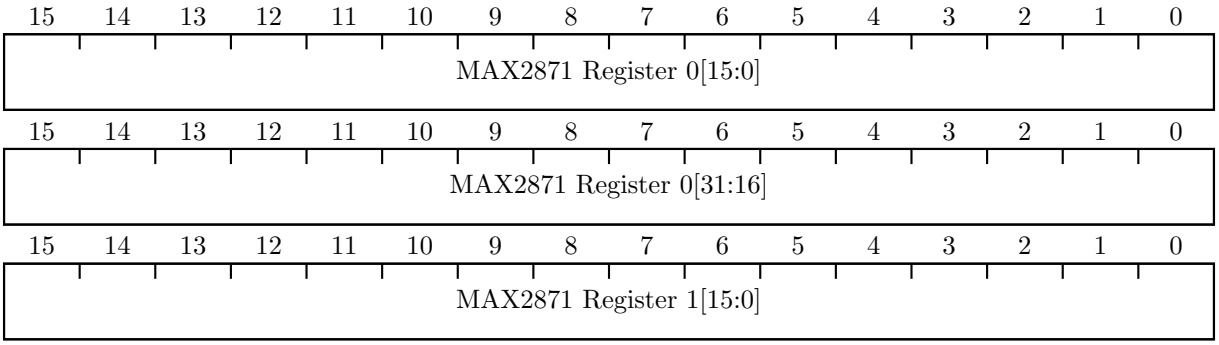
- **OWE:** Overwrite enable. If 1, this register is used to configure the hardware. If 0, all other bits in the register are ignored. Must be set to 0 for valid sweep operation.
- **Attenuator[6:0]:** Attenuator setting
- **SourceFilter:** Low pass filter selection for source signal

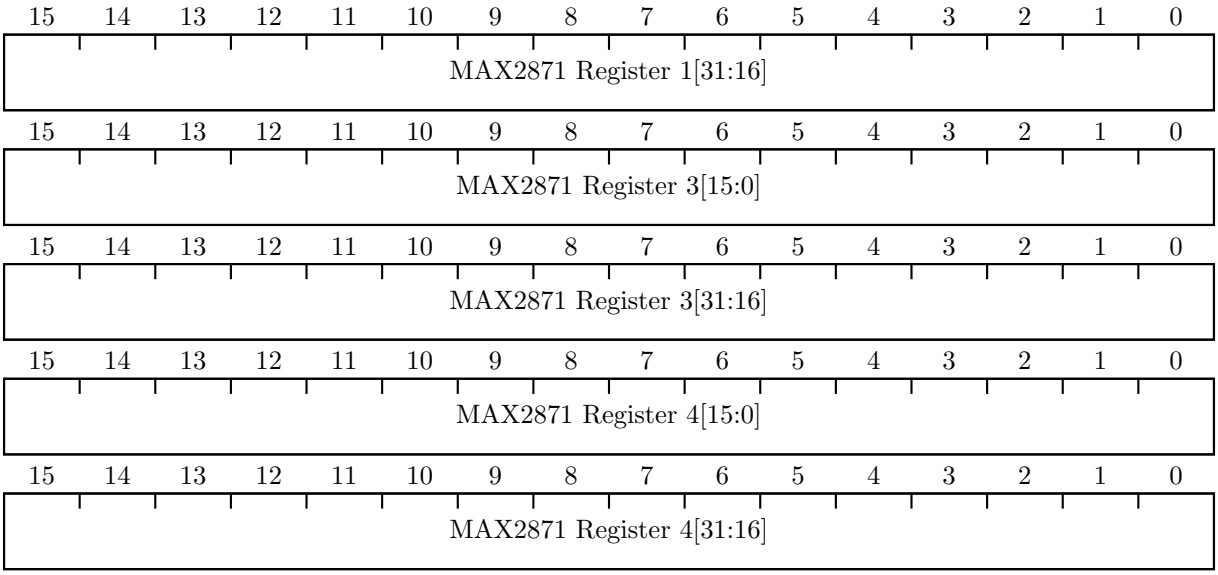
Setting	Selected Band
00	0 MHz to 900 MHz
01	900 MHz to 1800 MHz
10	1800 MHz to 3500 MHz
11	3500 MHz to 6000 MHz

- **BS: Band select.** Set to 0 for highband, set to 1 for lowband.
- **P1EN:** Route signal to port 1. Must not be enabled at the same time as P2EN.
- **P2EN:** Route signal to port 2. Must not be enabled at the same time as P1EN.

3.9 MAX2871 Default Values Registers: 0x08-0x0F

See datasheet of MAX2871 for bit descriptions. Bits for the fields N, FRAC, M, VCO and DIV_A are "don't care" as they will be overwritten by the SweepConfig setting.



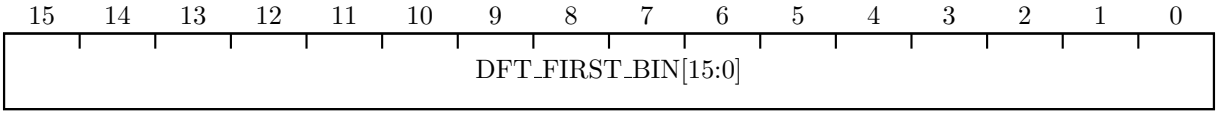


3.10 DFT registers

In addition to the single bin DFT configured through the ADC prescaler and phase increment registers (see 3.5 and 3.6), the FPGA also includes a multiple point DFT. This DFT only operates on the port 1 and port 2 receivers and is intended to speed up spectrum analyzer measurements. If enabled, the DFT runs in parallel to all other calculations.

The DFT has a fixed number of bins (96), but the frequencies these bins correspond to can be changed.

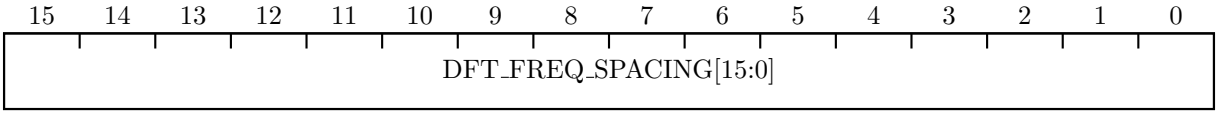
3.10.1 DFT_FIRST_BIN: 0x12



- **DFT_FIRST_BIN[15:0]:** This value determines the frequency corresponding to the first DFT bin.

$$f_{firstBin} = \frac{SR_{ADC} * DFT\_FIRST\_BIN}{2^{16}}$$

3.10.2 DFT_FREQ_SPACING: 0x13

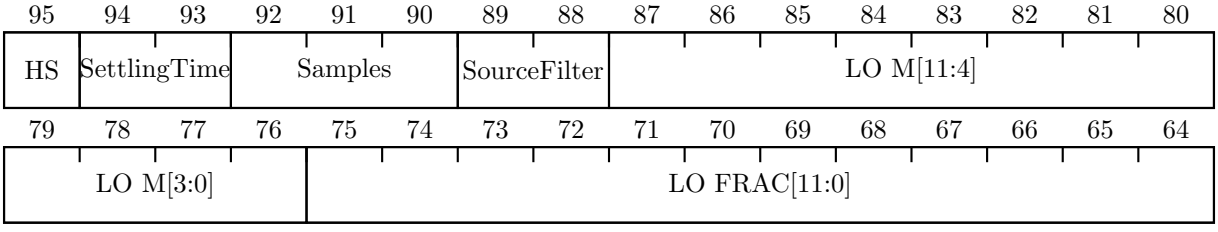


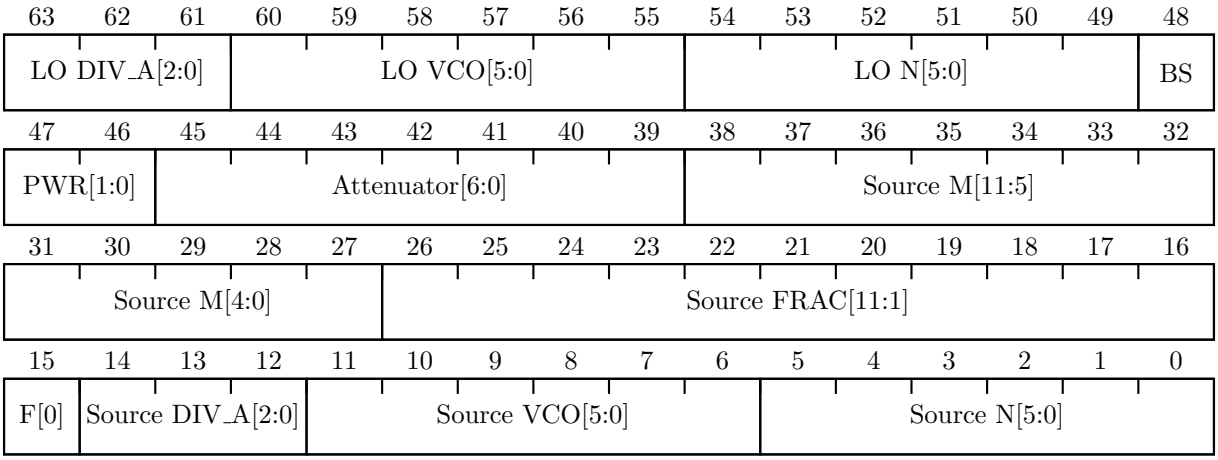
- **DFT_FREQ_SPACING[15:0]:** This value determines the frequency difference between bins.

$$\Delta f = \frac{SR_{ADC} * DFT\_FREQ\_SPACING}{2^{24}}$$

4 SweepConfig

The SweepConfig contains data for the source and LO1 PLL as well as the attenuator and source filter. Each point in the sweep, needs a valid SweepConfig before the sweep is started.





- **HS: Halt sweep.** If set, settling and sampling of this sweep point will be postponed until the sweep resume command is issued.
- **SettlingTime:** Amount of time between locking of PLLs and beginning of ADC sampling

Setting	Time
00	20 µs
01	60 µs
10	180 µs
11	540 µs

- **Samples:** Number of ADC samples to take

Setting	Samples	Equivalent IF bandwidth
000	Defined by SPP register	914 kHz/SPP
001	96	10 kHz
010	304	3 kHz
011	912	1 kHz
100	3040	300 Hz
101	9136	100 Hz
110	30464	30 Hz
111	91392	10 Hz

- **SourceFilter:** Low pass filter selection for source signal

Setting	Selected Band
00	0 MHz to 900 MHz
01	900 MHz to 1800 MHz
10	1800 MHz to 3500 MHz
11	3500 MHz to 6000 MHz

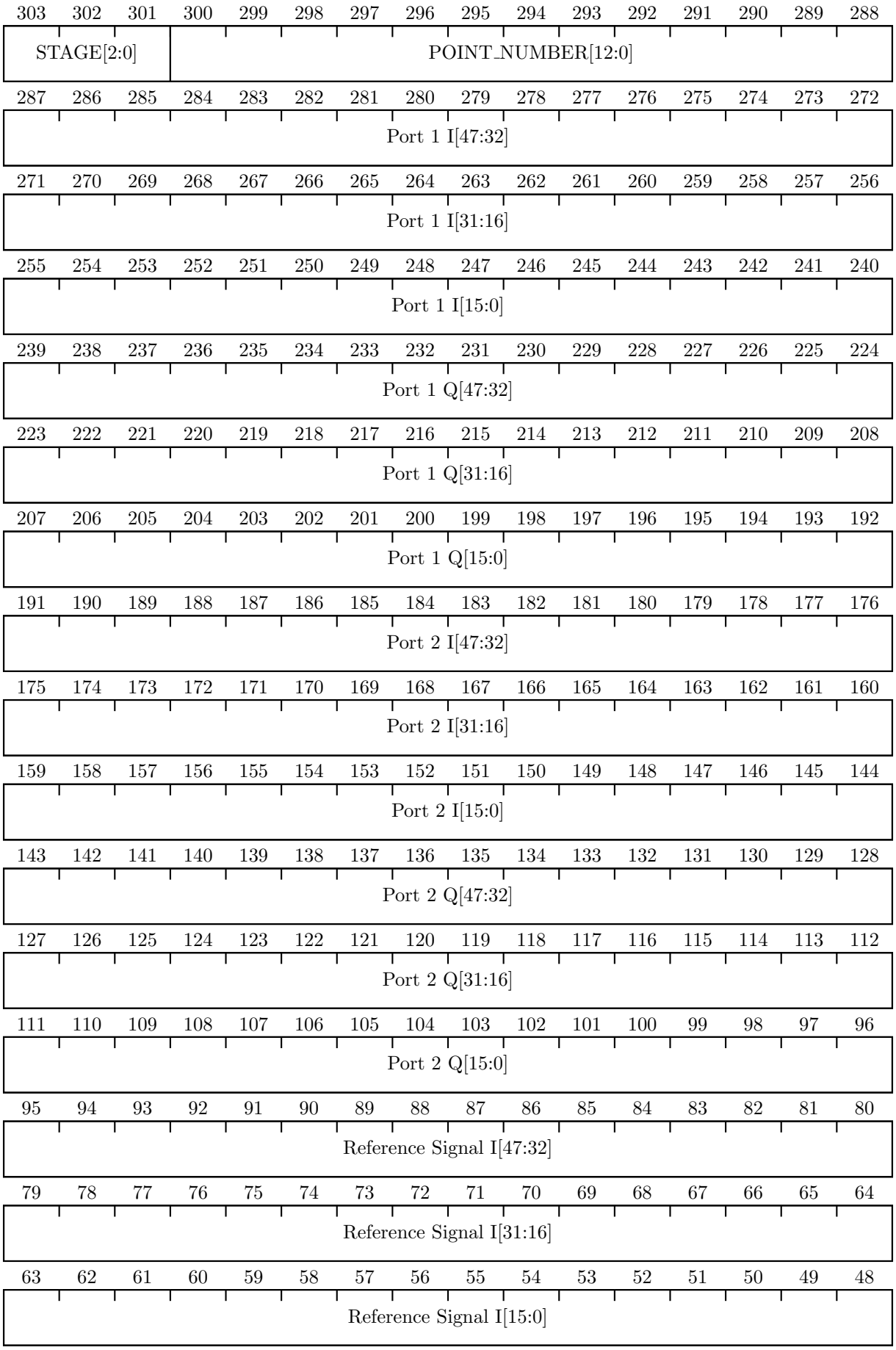
- **BS: Band select.** Set to 0 for highband, set to 1 for lowband.
- **PWR:** Power setting of source PLL. Will be written to register 4, bits [4:3] of the source PLL, controlling the output power of output A.

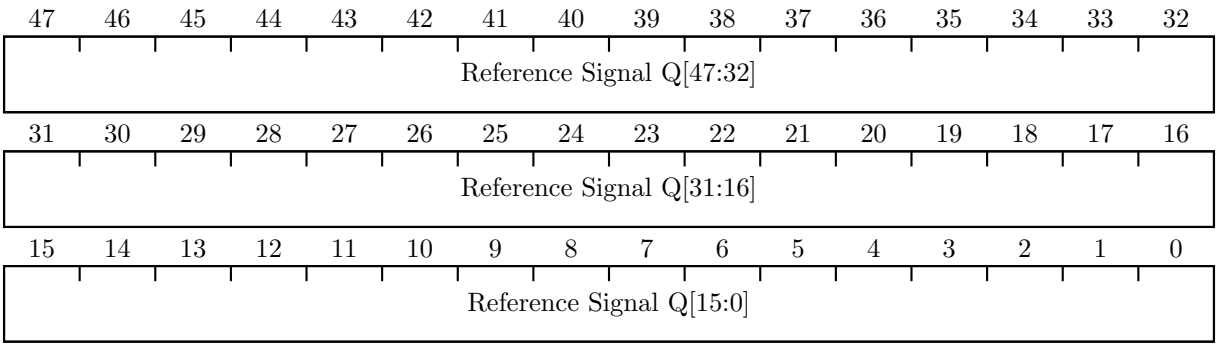
Setting	Selected Power
00	−4 dBm
01	−1 dBm
10	2 dBm
11	5 dBm

- **Attenuator:** Attenuation of source signal in 0.25 dB.

5 Sampling Result

Each point in the sweep generates a sampling results for each stage (see section 3.7).





6 Synchronization

The FPGA supports synchronization of the sweep across multiple devices. This feature can be enabled by setting the SYNC bit in the sweep setup register (see section 3.7). When enabled, the following conditions must be met:

- All participating devices must be connected in a loop via the trigger input and output pins. The order of the devices is not important.
- All devices must use the same sweep settings with the exception of the "Port 1 stage" and "Port 2 stage" settings in the sweep setup register.
- The port stages must be configured in such a way, that for each stage exactly one port is active in one device.

The synchronization works by delaying sampling until the stimulus signal is present, even when generated by another device. For each sampling stage, performs the following steps:

- When the device generates the stimulus signal in the current phase:
  - Set up source and 1.LO PLLs
  - If applicable: wait for the "resume sweep" command
  - Set the trigger output to high
  - Wait for high level on trigger input
  - Sample ADCs
  - Set the trigger output to low
  - Wait for low level on trigger input
- When the device does not generate the stimulus signal in the current phase:
  - Set 1.LO PLL
  - If applicable: wait for the "resume sweep" command
  - Wait for high level on trigger input
  - Set trigger output to high
  - Sample ADCs
  - Wait for low level on trigger input
  - Set the trigger output to low