1 Digital Interface

Pin	Direction	Function
SCK	in	SCK for SPI communication/SCK for PLL communication
MOSI	in	MOSI for SPI communication/MOSI for PLL communication
MISO	out	MISO for SPI communication/MUX for PLL communication
NSS	in	Chip Select for SPI communication/LE for PLL communication
INTR	out	Active high interrupt indicator
RESET	in	FPGA reset
AUX1	in	Selector for direct communication with Source PLL
AUX2	in	Selector for direct communication with LO PLL
AUX3	in	Active low modulation enable. Should be high when changing settings

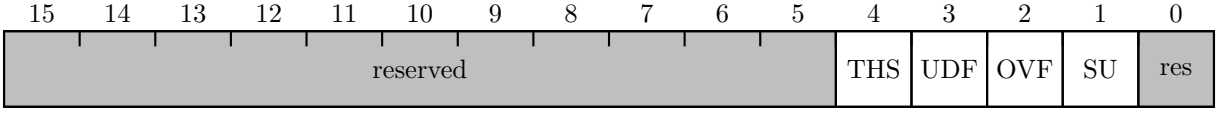
Depending on the voltage on AUX1/AUX2 the SPI port controls either the FPGA or one of the MAX2871 PLLs:

AUX1	AUX2	Function
low	low	SPI communication with FPGA
high	low	Direct feedthrough of SCK, MOSI, MISO and NSS to Source PLL
low	high	Direct feedthrough of SCK, MOSI, MISO and NSS to LO PLL
high	high	Invalid

When communicating with a PLL, the MUX output of the MAX2871 is forwarded to MISO and the NSS signal is forwarded to the LE pin. As the LE pin should stay low until after a valid register has been shifted in (see MAX2871 datasheet), set NSS low before switching to PLL communication mode.

2 SPI Protocol

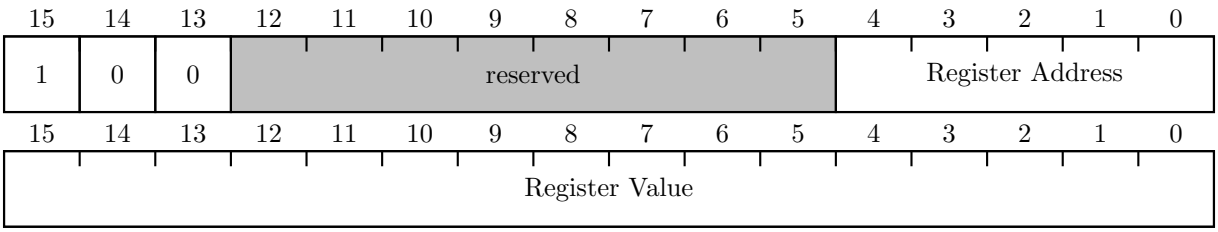
Each SPI transfer starts with pulling NSS low and ends with NSS returning to high level. SPI communication is done in words of 16 bits. The first word after NSS is pulled low is the command word and determines the amount and meaning of the following words. The word received while transmitting the command word is the interrupt status register:



- **THS:** Threshold of modulation FIFO reached. See also section 2.3. Reset on its own when the FIFO level drops again.
- **UDF:** Modulation FIFO underflow. Last sample will be used for modulation until new data arrives. Reset as a new sample is added to the FIFO.
- **OVF:** Modulation FIFO overflow. Oldest sample will be overwritten. Reset by disabling the modulation.
- **SU:** Source unlocked

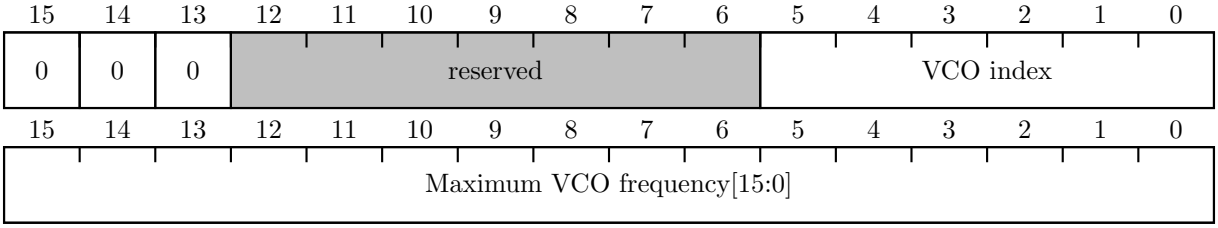
2.1 Writing a register

Writing a register requires the transfer of two words: First the control word selecting the destination address and a second word containing the new register value:



2.2 Writing the VCO lookup table

The MAX2871 contains 64 individual VCOs. The correct VCO has to be selected for each frequency. During modulation, the FPGA performs the VCO selection and needs to know the frequency limits for each VCO. It contains a lookup table with a 16-bit entry for each VCO. This table has to be filled before enabling the modulation, as each MAX2871 sample has slightly different VCO limits (see MAX2871 datasheet for algorithm to determine the limits). Updating a table entry is done by sending two SPI words:



The maximum VCO frequency is given in terms of the MAX2871 reference frequency. It is a Q10 fixed point integer.

$$MaximumVCOfrequency[15:0] = \frac{f_{max} * 1024}{f_{reference}}$$

Example: With a reference frequency $f_{reference} = 104MHz$ and a maximum usable frequency of the VCO of $f_{max} = 3718MHz$, set the maximum VCO frequency value to 36608.

2.3 Modulation FIFO handling

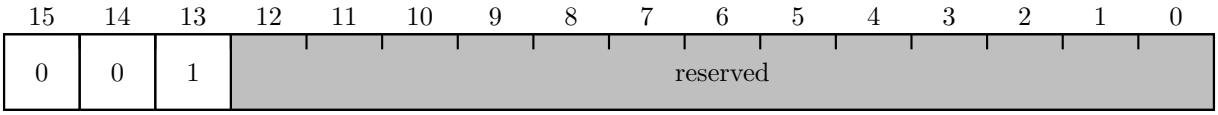
The modulation module contains a data FIFO for the modulation data (samples). Each sample is an 8-bit word that determines the modulation state. The modulation moves on to the next sample at a rate determined by MOD_PHASE_INC. The FIFO has a size of 2048 samples. It can only be written to, reading back data from the FIFO is not possible.

The FIFO also has three interrupts (see status register, section refreg:status):

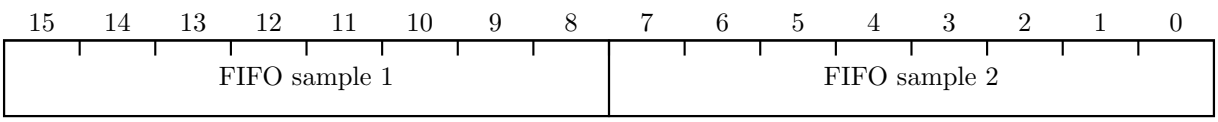
- **Overflow:** Asserted when samples have been written to an already full FIFO. This bit does not clear even if the FIFO level drops afterwards. The modulation has to be disabled to reset this bit. Disabling the modulation also clears the FIFO.
- **Underflow:** Asserted when no more samples are available in the FIFO but the modulation module is scheduled to move to the next sample. The modulation will continue to use the last available sample until new data is written to the FIFO. This bit is cleared by writing new FIFO data.
- **Threshold crossed:** Asserted when the FIFO contains at least MOD_FIFO_THRESHOLD (see section refreg:mod:fifo:thresh) samples.

2.3.1 Writing to the modulation FIFO

It is only possible to write to bytes at a time to the modulation FIFO. Initiate the write by sending the command word:



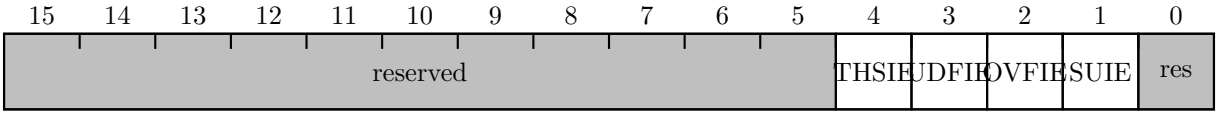
Follow up the same SPI transaction (NSS has to stay low) with as many words as desired, each word containing two FIFO samples:



FIFO sample 1 is added to the FIFO first, followed by FIFO sample 2.

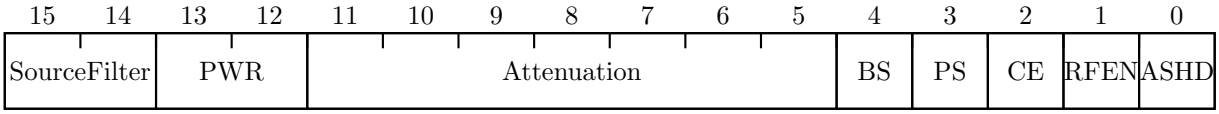
3 Registers

3.1 Interrupt Mask Register: 0x00



- **THSIE:** FIFO threshold crossed interrupt enable
- **UDFIE:** FIFO underflow interrupt enable
- **OVFIE:** FIFO overflow interrupt enable
- **SUIE:** Source unlocked interrupt enable

3.2 Source Control Register: 0x01



- **SourceFilter:** Low pass filter selection for source signal

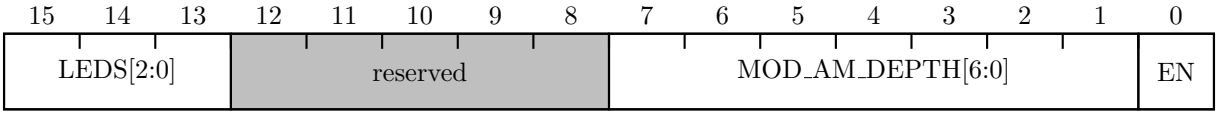
Setting	Selected Band
00	0 MHz to 900 MHz
01	900 MHz to 1800 MHz
10	1800 MHz to 3500 MHz
11	3500 MHz to 6000 MHz

- **PWR:** Power setting of source PLL. Will be written to register 4, bits [4:3] of the source PLL, controlling the output power of output A.

Setting	Selected Power
00	−4 dBm
01	−1 dBm
10	2 dBm
11	5 dBm

- **Attenuator:** Attenuation of source signal in 0.25 dB.
- **BS: Band select.** Set to 0 for highband, set to 1 for lowband.
- **PS: Port select.** Set to 0 for Port 1, set to 1 for Port 2.
- **CE: Source chip enable.**
- **RFEN: Source RF enable.**
- **ASHD: Amplifier disable.**

3.3 Modulation control register: 0x02

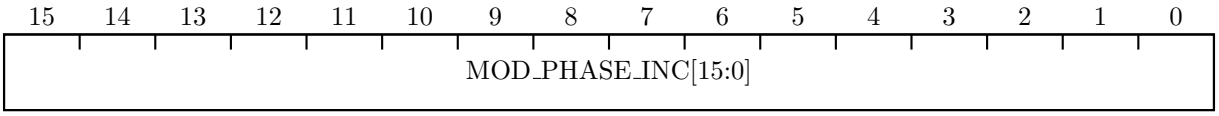


- **LEDS:** User LED status:

LED num	Function
0	Debug
1	Ready
2	Ext. reference

- **MOD_AM_DEPTH:** Depth of amplitude modulation. Higher values of the modulation sample result in deeper modulation. This setting determines the maximum depth. 127 is equivalent to 100% modulation.
- **EN: Enable modulation.** Set to 1 to enable the modulation. For the modulation to actually start, AUX3 also has to be pulled low. Set to 0 to disable the modulation (when changing settings or to clear the modulation FIFO).

3.4 Modulation phase increment register: 0x03

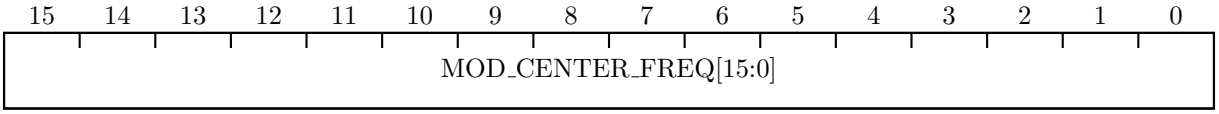


Determines the rate at which the modulation module consumes samples:

$$f_{sample} = \frac{104MHz * MOD\_PHASE\_INC}{2^{27}}$$

Example: set to 25811 for a sample rate of approximately 20 kHz.

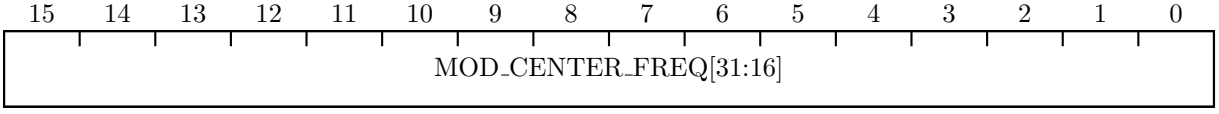
3.5 Modulation center frequency LSB register: 0x04



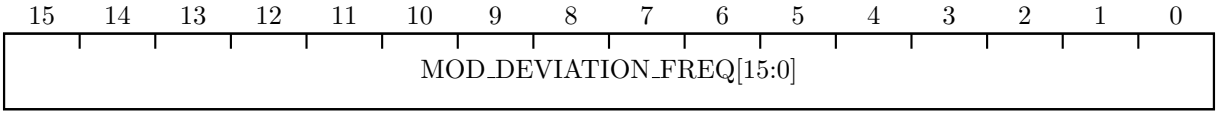
- **MOD_CENTER_FREQ[32:0]:** See also other registers for remaining bits (sections 3.6 and 3.8). Sets the center frequency of the frequency modulation. It is given in terms of the MAX2871 reference frequency. It is a Q27 fixed point integer.

$$MOD\_CENTER\_FREQ[32:0] = \frac{f_{center} * 2^{27}}{f_{reference}}$$

3.6 Modulation center frequency MSB register: 0x05



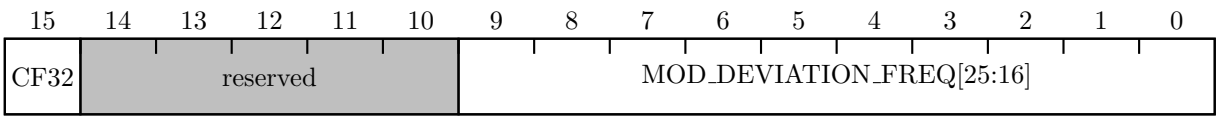
3.7 Modulation deviation frequency LSB register: 0x06



- **MOD_DEVIATION_FREQ[25:0]:** See also other register for remaining bits (section 3.8). Sets the maximum deviation from the center frequency during frequency modulation. It is given in terms of the MAX2871 reference frequency. It is a Q27 fixed point integer. As it only has 26 bits, the maximum deviation is half the reference frequency.

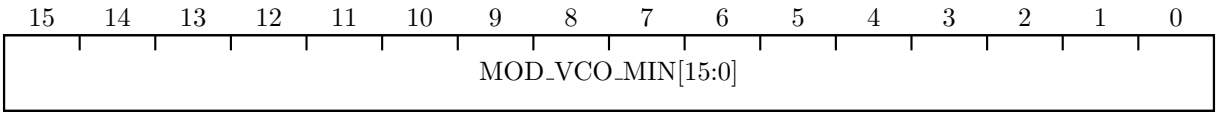
$$MOD\_DEVIATION\_FREQ[25:0] = \frac{f_{max_deviation} * 2^{27}}{f_{reference}}$$

3.8 Modulation deviation frequency MSB register: 0x07



- **CF32:** Most significant bit of MOD_CENTER_FREQ.

3.9 Minimum VCO frequency LSB register: 0x08

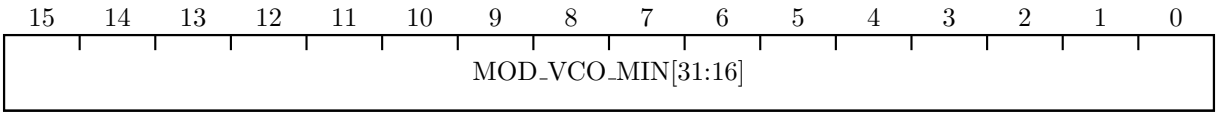


- **MOD_VCO_MIN[31:0]:** See also other register for remaining bits (section 3.10). Sets the minimal allowed undivided VCO frequency. Used to determine the VCO divider when changing frequencies. It is given in terms of the MAX2871 reference frequency. It is a Q27 fixed point integer. Always set this for a minimal undivided VCO frequency of 3 GHz.

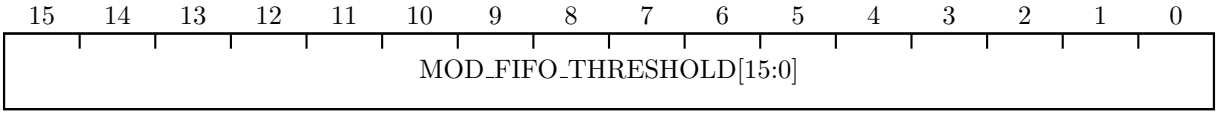
$$MOD\_VCO\_MIN[31:0] = \frac{f_{min_vco} * 2^{27}}{f_{reference}}$$

For the default reference frequency of 104 MHz, set this value to 3871665231.

3.10 Minimum VCO frequency MSB register: 0x05



3.11 Modulation FIFO threshold register: 0x0A



- **MOD_FIFO_THRESHOLD[15:0]:** Number of samples in the FIFO after which the FIFO threshold interrupt is asserted.